Claim 21 should be replac d with:

21. (Amended) A FPGA-based SoC development and verification system, the system comprising:

a software core for a logic analyzer inserted within the FPGA-based SoC during customization of the FPGA-based SoC;

an external software monitor tool having an interface for communicating with said logic analyzer software core; and

a communication port for facilitating exchange of data between said logic analyzer software core and said external monitor tool.

Please add Claims 29-37 as follows:

29. (New) A method for developing and verifying a FPGA-based SoC within a system, the method comprising:

executing software code for a logic analyzer located within the FPGA-based SoC, the software code being the core software code for the logic analyzer;

defining at least one monitor probe point within the FPGA-based SoC for analysis by the logic analyzer, wherein the software code and the at least one monitor probe point defined are created during customization of the FPGA-based SoC; and

collecting information for the at least one monitor probe point to facilitate analysis of signals within the system while developing and verifying the FPGA-based SoC.

30. (New) The method of claim 29, wherein the system further includes a microprocessor coupled to the FPGA-based SoC.

31. (New) The method of claim 29, wherein the FPGA-based SoC is an FPGA-based embedded processor SoC.

32. (New) A machine readable storage having stored thereon, a computer program having a plurality of code sections, the code sections executable by a machine for causing the machine to perform the steps of:

executing software code for a logic analyzer located within an FPGA-based SoC portion of a system, the software code being the core software code for the logic analyzer utilized for developing and verifying the FPGA-based SoC;

defining at least one monitor probe point within the FPGA-based SoC for analysis by the logic analyzer, wherein the software code and at least one monitor probe point defined are created during customization of the FPGA-based SoC; and

collecting information for the at least one monitor probe point to facilitate analysis of signals within the system while developing and verifying the FPGA-based SoC.

33. (New) The machine readable storage of claim 32, wherein the system further includes a microprocessor coupled to the FPGA-based SoC.

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34. (New) The machine readable storage of claim 32, wherein the FPGA-based SoC is an FPGA-based embedded processor SoC.

35. (New) A GUI for development and verification of a system including an FPGA-based SoC, the GUI comprising:

a selection dialog for defining and selecting monitor probe points within the system, the monitor probe points being located within the FPGA-based SoC;

a display window for displaying waveforms for trace and trigger conditions; and

a communication interface for facilitating communication with a logic analyzer core integrated within the FPGA-based SoC.

36. (New) The GUI of claim 35, wherein the system further includes a microprocessor coupled to the FPGA-based SoC.

37. (New) The GUI of claim 35, wherein the FPGA-based SoC is an FPGA-based embedded processor SoC.